REMARKS

Claims 1-18 are pending in the present application. Reconsideration and allowance of pending claims 1-18 in view of the following remarks are requested.

A. Examiner's Request for Formal Drawings

In response to the Examiner's request for formal drawings, Applicant has submitted herewith two (2) replacement sheets which include formal drawings of all Figures 1- 4. Two (2) clean sheets of formal drawings are also included herewith.

B. Rejection of Claims 1-18 under 35 USC §103(a)

The Examiner has rejected claims 1-18 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,343,434 to Kenji Noguchi ("Noguchi") and further in view of U.S. patent number 5,646,948 to Kobayashi et al. ("Kobayashi"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 10, is patentably distinguishable over Noguchi and Kobayashi, singly or in combination thereof.

The present invention, as defined by independent claim 1, includes, among other things, measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device

passes or fails an erase test by using the first test limit and the second test limit during the erase test. As disclosed in the present application, conventional flash memory test procedures use a single test limit against which uniform and non-uniform size sectors are compared, which results in a large number of false rejects. As disclosed in the present application, to overcome the above problem, the present invention includes measuring at least one time period related to erasing a first sector having a first sector type, such as a uniformly sized sector, and establishing a first test limit based in part on the first time period.

As disclosed in the present application, the present invention also includes measuring at least one second time period related to erasing a second sector having a second sector type, such as a boot sector, and establishing a second test limit based at least in part on the second time period. As disclosed in the present application, one sector type generally has a different memory size than another sector type. By way of example, boot sectors are generally smaller than uniform sectors. As disclosed in the present application, the first and second test limits, which are associated with respective first and second sectors having first and second sector type memory sizes, are used to determine whether the memory device passes or fails an erase test. Thus, the present invention advantageously achieves a method for testing a flash memory device having first and second sectors of respective first and second type memory sizes, where first and second test limits, which correspond to respective first and second sectors, are used to determine whether the device passes or fails an erase test. As a result, the present invention

advantageously reduces the number of false rejects compared to a conventional approach that uses only a single test limit to test sectors having different sector type memory sizes.

In contrast to the present invention as defined by independent claim 1, Noguchi does not teach, disclose, or suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. Noguchi is directed to a method for reducing the rate at which fail products are produced by use of a flash memory which is determined as fail because of the presence of an over-erased memory cell as a one-time programmable memory device. See, for example, the Abstract of Noguchi. Noguchi specifically discloses an erasing operation of a nonvolatile semiconductor memory device where, in an erase cycle, if memory cell data is unerased, an erase pulse width TEW is incremented and an erasing sequence is repeated. See, for example, column 7, lines 7-8, column 8, lines 9-11, and Figure 14 of Noguchi.

In Noguchi, the erase operation includes erasing memory cells in a memory array. However, Noguchi fails to teach, disclose, or remotely suggest a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size. In fact, Noguchi does not even mention different sectors having different sector type memory sizes. Also, Noguchi fails to teach, disclose, or suggest

measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test, as specified in independent claim 1.

In contrast to the present invention as defined by independent claim 1, Kobayashi does not teach, disclose, or suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. Kobayashi is directed to a memory testing apparatus which is capable of concurrently testing a plurality of semiconductor flash memories in parallel. See, for example, Kobayashi, column 1, lines 11-15. Kobayashi specifically discloses a semiconductor memory test apparatus comprising timing generator 10, pattern generator 2, waveform shaper 3, logical comparing part 40, and all-pass detector (NOR gate) 43, which are used for testing "n" flash memories MUT_1, MUT_2, ... MUT_n that are in "n" test channels, respectively. See, for example, column 4, lines 31-44 and Figure 1 of Kobayashi.

However, Kobayashi fails to teach, disclose, or even suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test, as specified by independent claim 1. As discussed above, the present invention advantageously achieves a method for testing a flash memory device having first and second sectors of respective first and second type memory sizes, where first and second test limits, which correspond to respective first and second sectors, are used to determine whether the device passes or fails an erase test. However, Kobayashi does not even mention erase testing a flash memory device having first and second sectors with respective first and second sector memory sizes. In fact, Kobayashi does not even mention different sectors having different sector type memory sizes. Thus, Kobayashi fails to cure the basic deficiencies of Noguchi discussed above.

Furthermore, on pages 8 and 9 of the Office Action dated December 1, 2004, the Examiner states that incorporating the multiple memories of Kobayashi with the testing apparatus of Noguchi would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by applying the testing routine taught by Noguchi with multiple memory types would reduce overall testing time. However, as discussed above, the present invention advantageously reduces the number

of false rejects compared to a conventional approach that uses only a single test limit to test sectors having different sector type memory sizes. Applicant respectfully submits that the combination of Kobayashi and Noguchi as suggested by the Examiner does not teach, disclose, or remotely suggest using a first test limit to test first sectors having a first sector type memory size and using a second test limit to test second sectors having a second sector type memory size in an erase test for first and second sectors are in a semiconductor device, as specified in independent claim 1.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Noguchi and Kobayashi, singly or in combination. As such, independent claim 1 is patentably distinguishable over Noguchi and Kobayashi. Thus, claims 2-9 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 10, includes, among other things, a measuring element configured to measure a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, an establishing element configured to establish a first test limit and a second test limit based on the respective first time period and second time period, and a determining element configured to determine whether the device passes or fails an erase test by using the first test limit and the second test limit

during the erase test. Independent claim 10 includes similar limitations as independent claim 1 discussed above. Thus, for similar reasons as discussed above, independent claim 10 is also patentably distinguishable over Noguchi and Kobayashi. Thus, claims 11-18 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 10, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-18 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-18 pending in the present application is respectfully requested.

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Respectfully Submitted,
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